

1. A network switch comprising:
 - at least one port data port interface;
 - a first memory;
 - a second memory; and
 - a memory management unit in connection with said at least one data port interface, said first memory, and said second memory,

2. A network switch as recited in claim 1, said network switch further comprising

3. A network switch as recited in claim 1, said network switch further comprising

4. A network switch as recited in claim 1, wherein said first memory further comprises on-chip memory.

6. A network switch as recited in claim 1, wherein the memory management unit further comprises:

- a communication channel;
- a data input section in connection with the communication channel;
- a data output section in connection with the communication channel;
- a first memory controller in connection with the first memory, the data input

section, and the data output section;

unit; and

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13. A network switch as recited in claim 12, wherein the cell disassembly unit converts a cell format from a CBP format to a CP bus format and transmits a cell to the communication channel when enabled to do so.

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15. A network switch as recited in claim 14, wherein the predetermined algorithm

further comprises a token order.

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17. A network switch as recited in claim 7, wherein said at least one address pool

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a cell free address pool connected to the first memory controller; and

a slot free address pool connected to the second memory controller.

18. A network switch as recited in claim 6, said network switch further comprising:

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a scheduler connected to the first memory controller and the second memory controller.

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20. A network switch as recited in claim 19, wherein the cell free address pool controller is configured to receive and release free addresses from the cell free address pool unit for use in storing cells in the first memory.

22. A network switch as recited in claim 18, wherein the slot free address pool
unit

23. A network switch as recited in claim 22, wherein the slot free address pool controller is configured to receive and release free slots from the slot free address pool for use in storing cells in the second memory.

25. A network switch as recited in claim 18, wherein the second memory controller receives and processes requests for storage of data in the second memory.

27. A method for storing data in a network switch, said method comprising the steps of:

formatting the data received as a linked list:

and

storing the data in the first memory or the second memory based on the

determining step.

28. A method for storing data in a network switch as recited in claim 27, wherein the determining step further comprises the steps of:

determining if a cell count is less than a first predetermined threshold for the egress;

determining if a number of cells in the second memory is zero; and

determining if a number of cells in the first memory added to a number of cells remaining in an assembly is less than the first predetermined threshold.

29. A method for storing data in a network switch as recited in claim 27, wherein the step of storing data in the first memory further comprises the steps of:

initializing a cell count;

setting an in progress flag;

loading a first cell pointer into a memory controller;

incrementing the cell count;

storing a first cell in the local memory;.

30. A method for storing data in a network switch as recited in claim 29, further comprising the steps of

incrementing the cell count;

storing a next cell in the first memory;

determining if a last cell bit is set; and

loading a next cell pointer and continuing to store cells if the last cell bit is determined not to be set.

31. A method for storing data in a network switch as recited in claim 27, wherein the step of storing data in the second memory further comprises the steps of initializing global storage of data and continuing global storage of data until a last slot is stored.

32. A method for storing data in a network switch as recited in claim 31, wherein the step of initializing global storage further comprises the steps of:

initializing a global cell count and setting an in progress flag;

incrementing the global cell count;

writing a first cell to a cell accumulation buffer;

